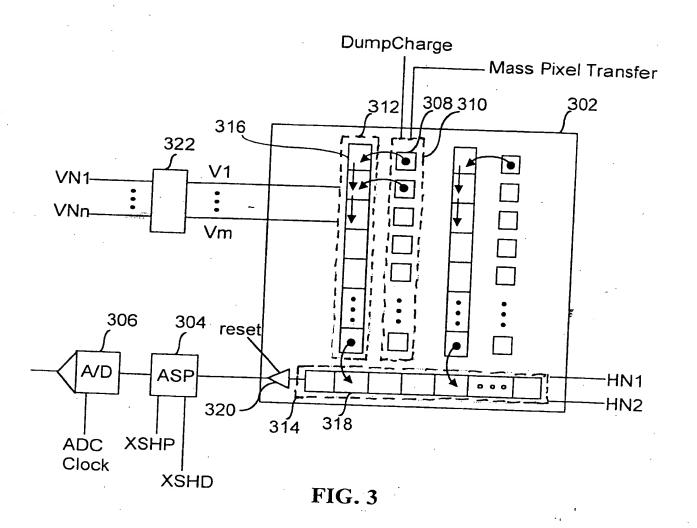
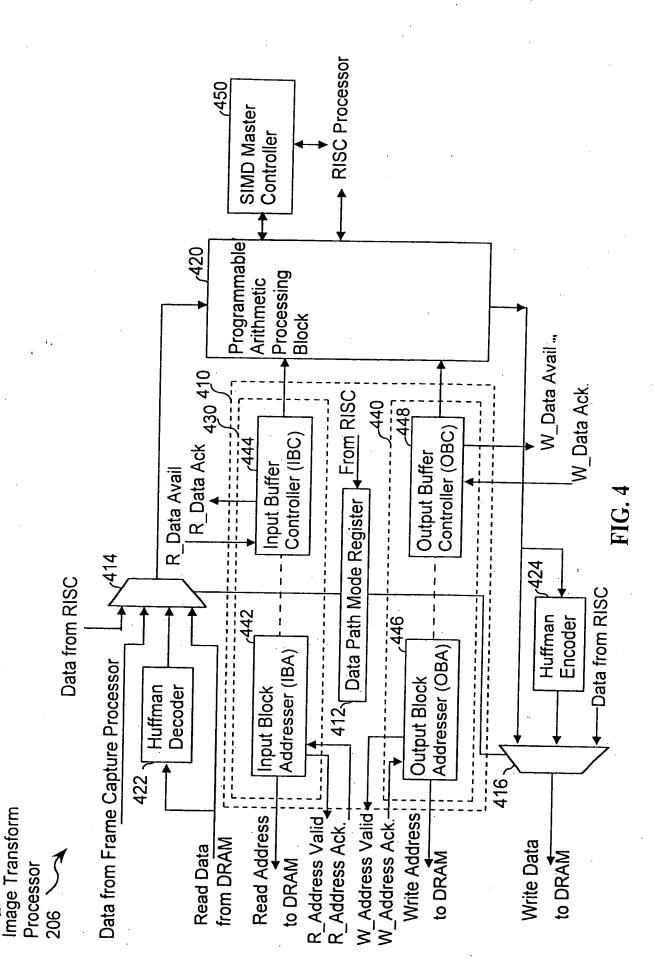


FIG. 2



Programable



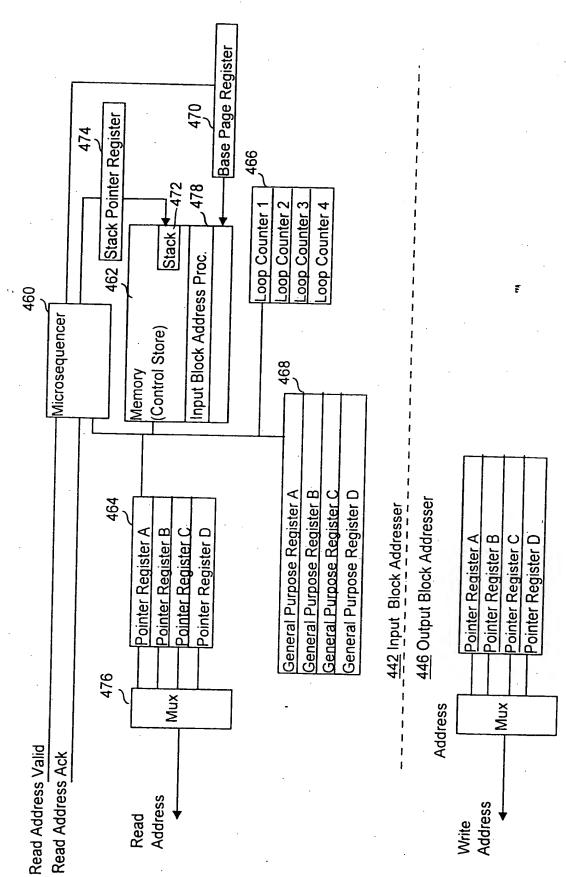
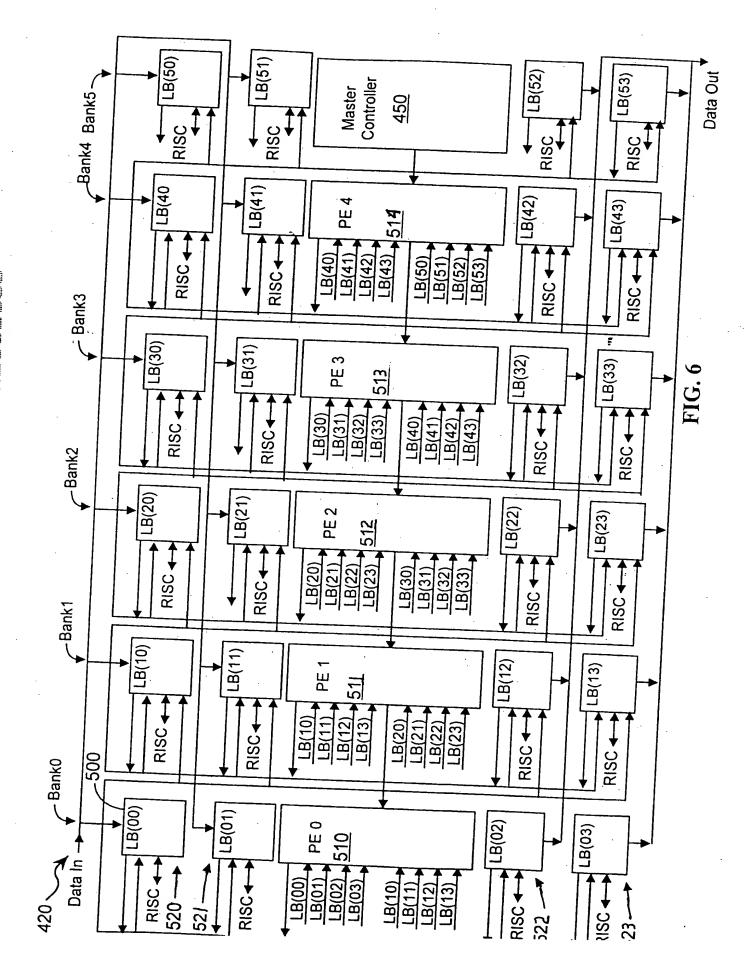
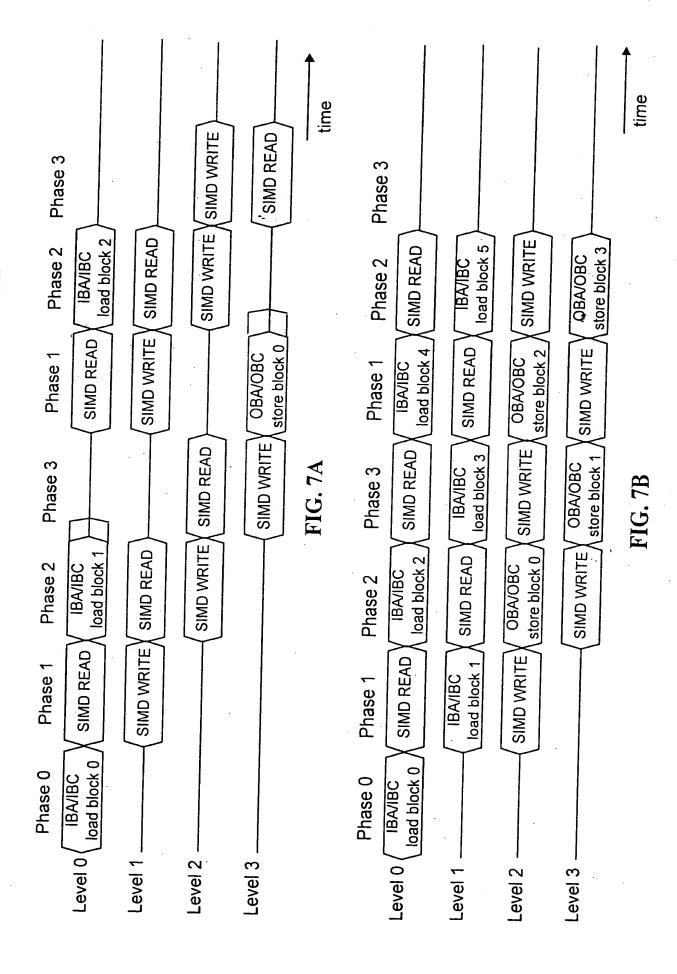


FIG. 5





580

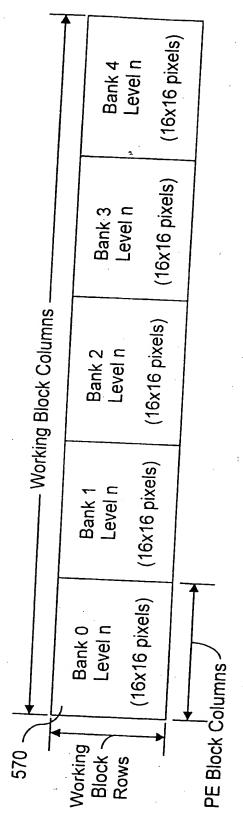


FIG. 8

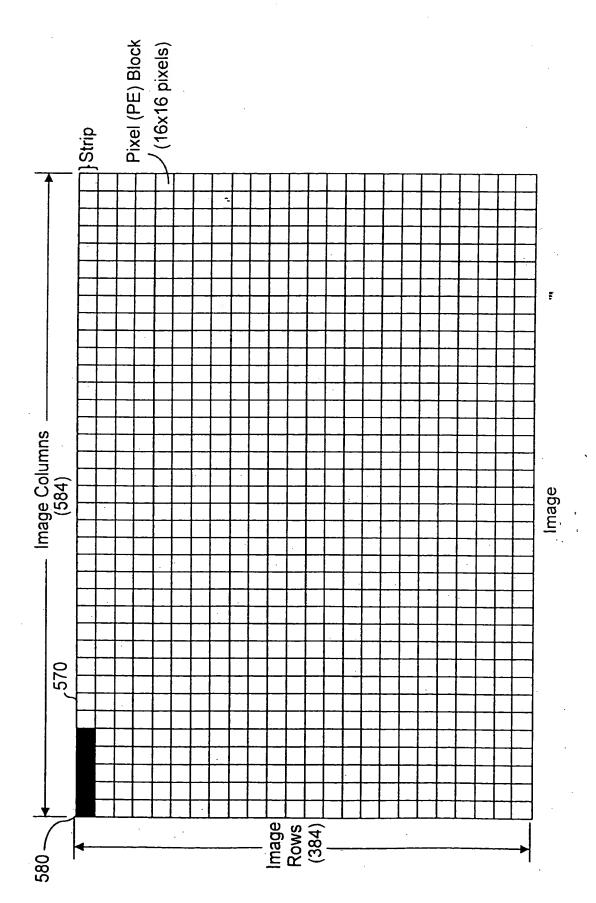
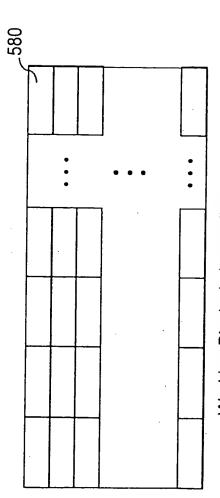
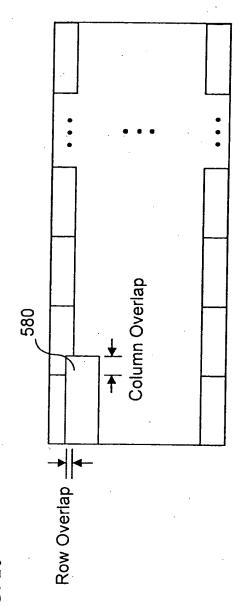


FIG.



Working Blocks in Image Data

FIG. 10



Overlapping Working Blocks in Image Data FIG. 11

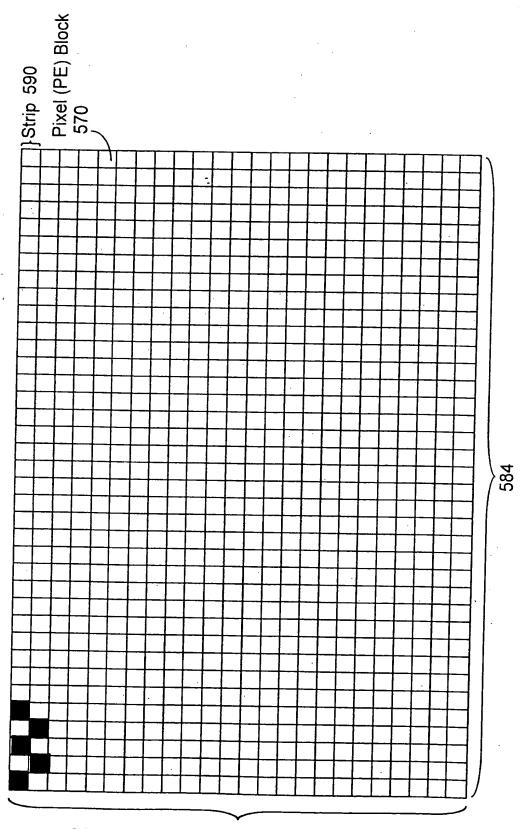


Image and Example of a dispersed processing blocks making up a working block.  ${
m FIG.~12A}$ 

以

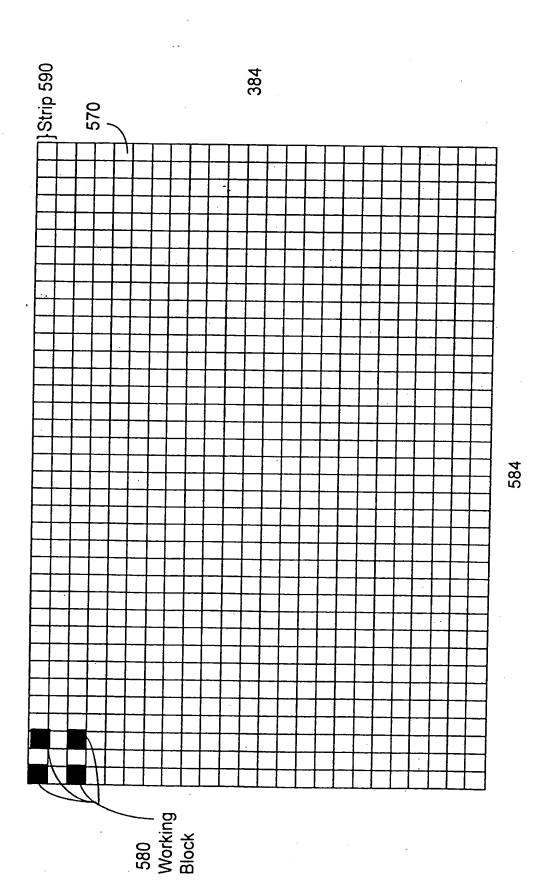


Image and Example of a dispersed processing blocks making up a working block.  ${f FIG.~12B}$ 

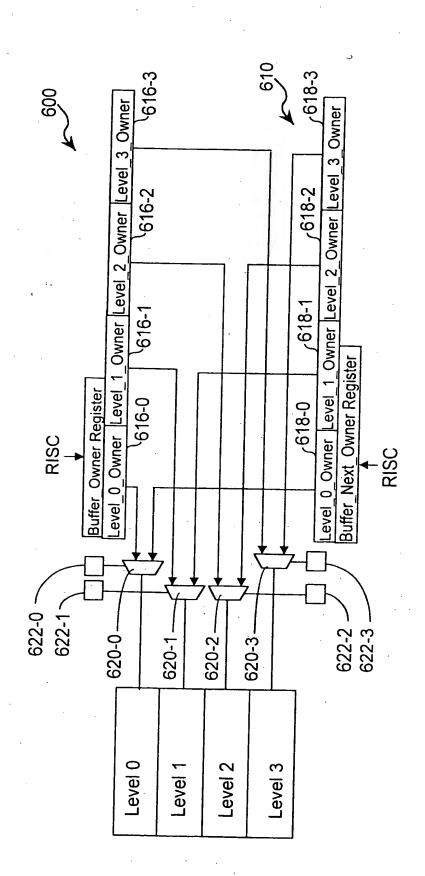


FIG. 13

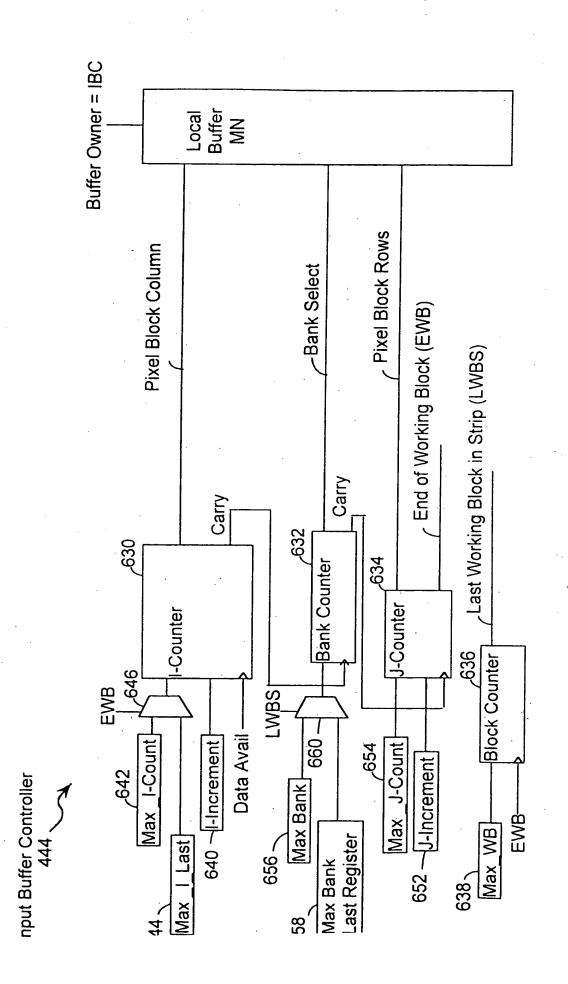
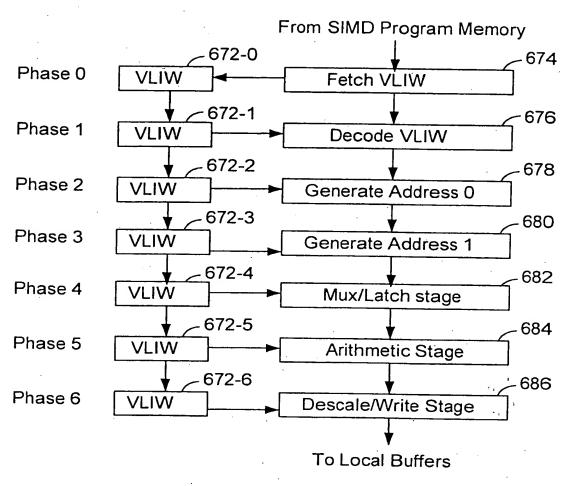
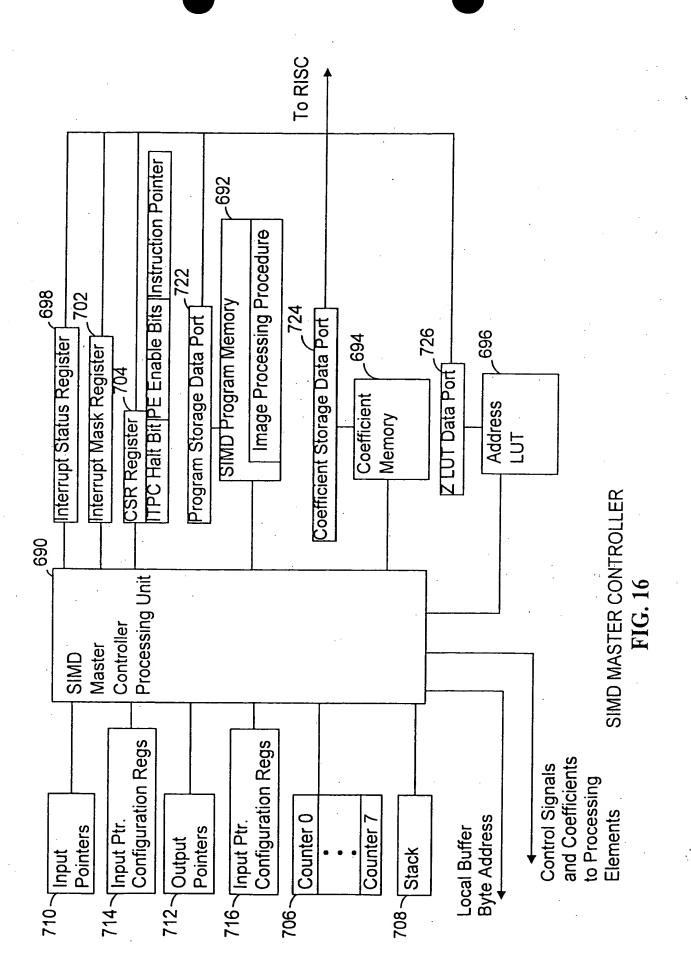


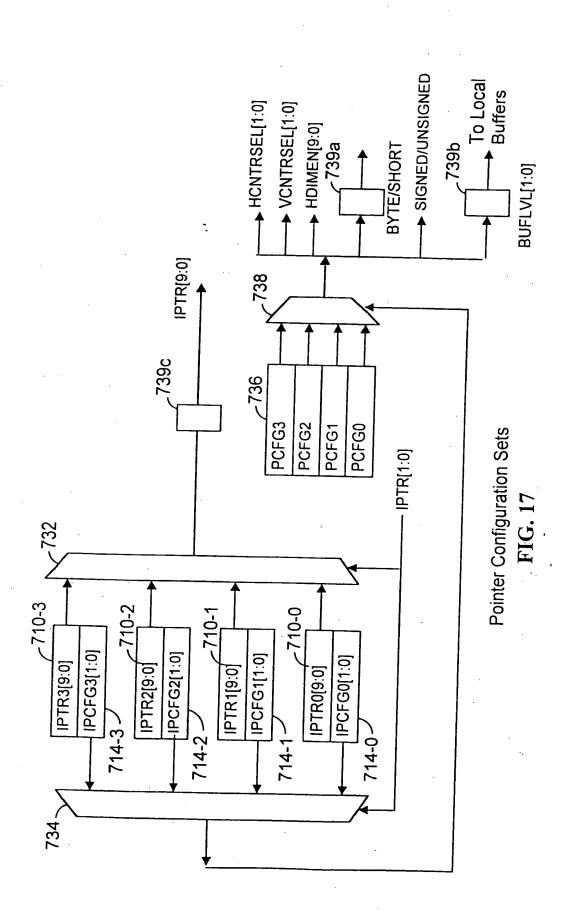
FIG. 14

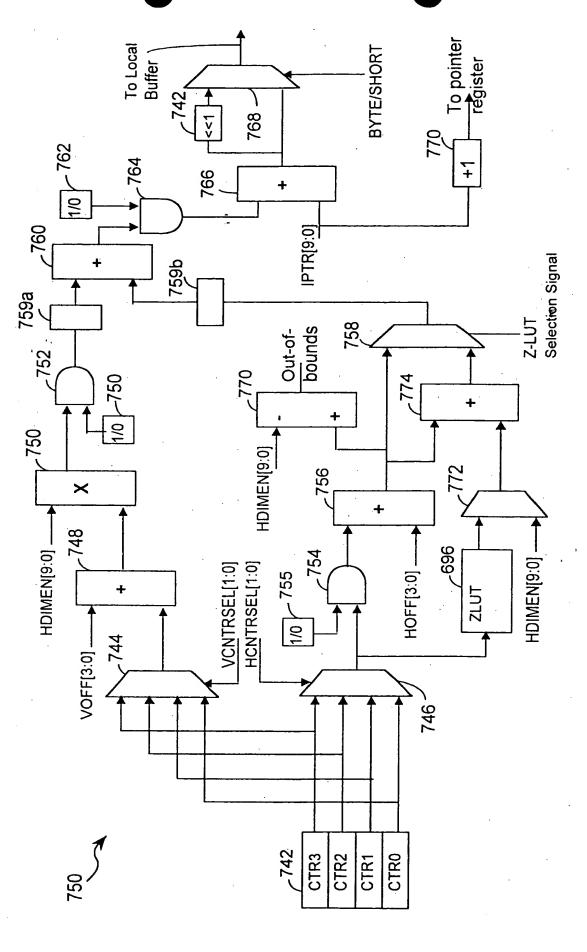
670



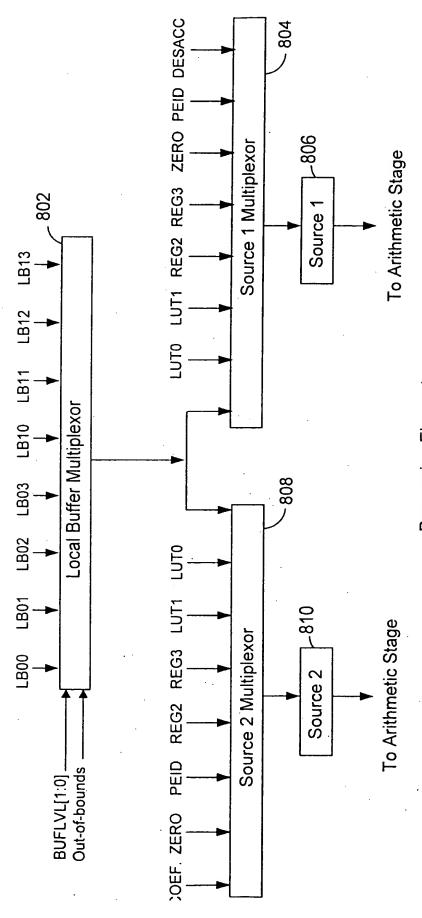
SIMD Pipeline Stages FIG. 15



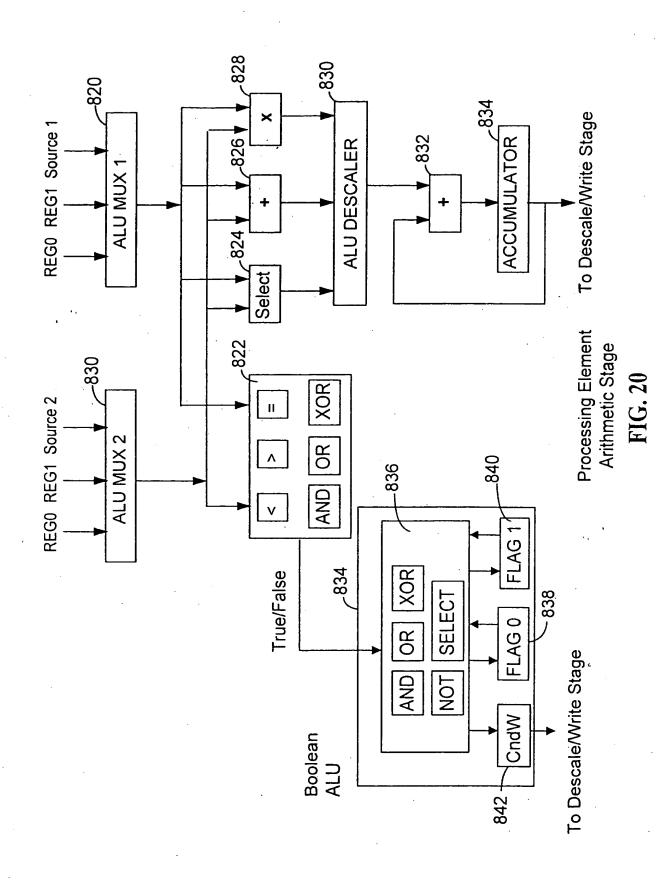


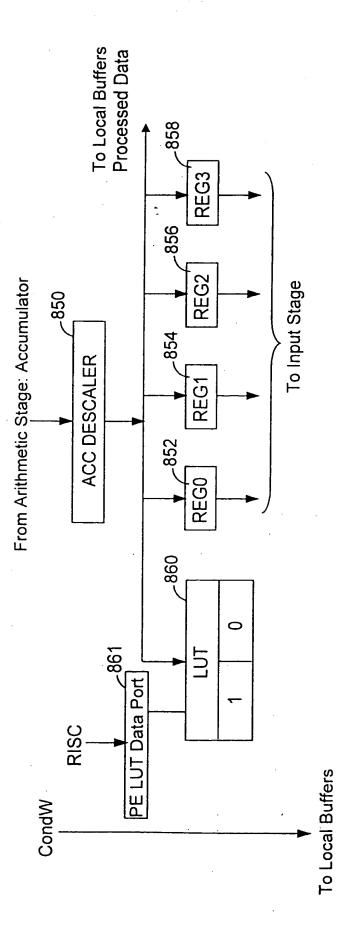


EFFECTIVE ADDRESS GENERATION FIG. 18



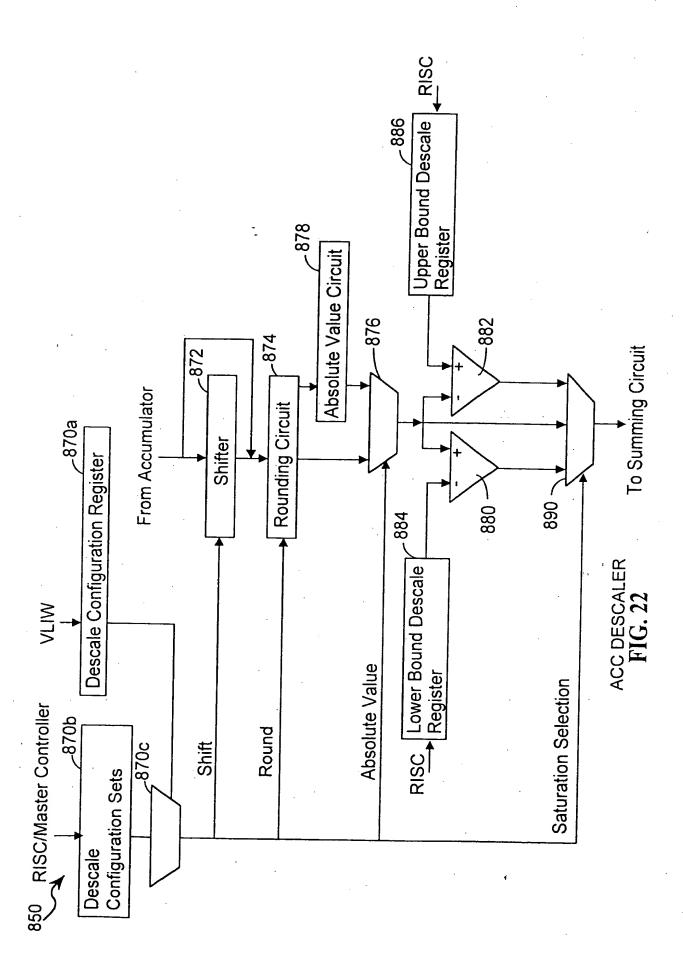
Processing Element
Multiplexor/Latch Stage
FIG. 19

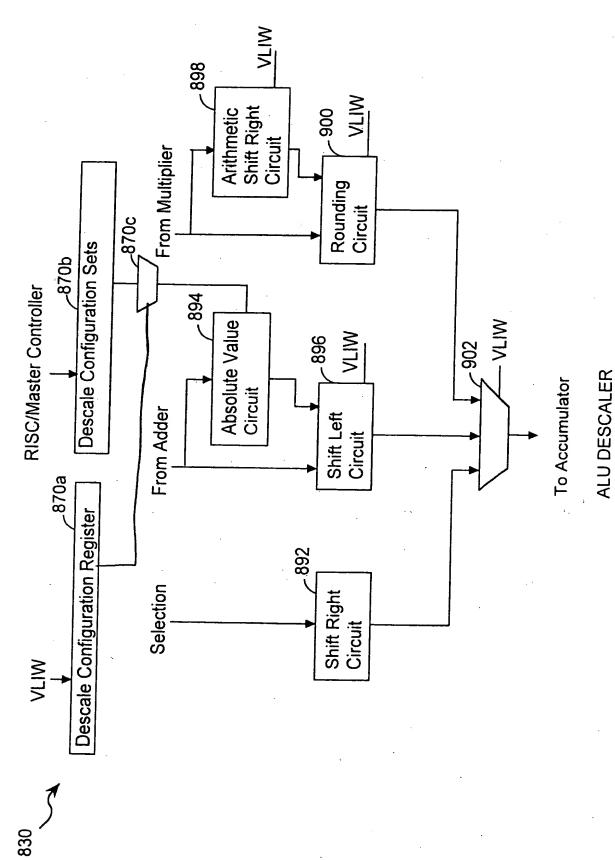




Processing Element Descale/Write Stage

**FIG. 21** 





ALU DESCALEI FIG. 23

